Architecturual internals

General architecture internals.

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General architecture

The Mirocom Broadband Engine (M/BE) is a low-power heterogeneous system-on-chip (SoC) aimed at targeting embedded systems as well as general purpose applications with moderate resource utilization.

Terminology

APE):
: An application processing element (APE) is a RISC-V core / unit of execution that is capable of executing MISA instructions from memory.

SPE):
: A synergistic processing element (SPE) is a specialized co-processor used for vectored and floating point operations and is connected to the APEs through the element interconnect bus (EIB).

EIB):
: An element interconnect bus connects SPEs and APEs.

MISA):
: The Mirocom Instruction Set Architecture (MISA) is the native instruction set understood by APEs.

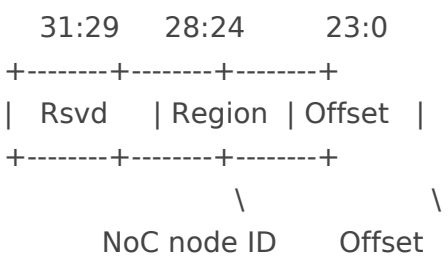
Zero-relative addressing

During a memory operation within M/BE SoC, a memory address will be used to locate data in memory or in device-register address space. Unlike with typical memory addressing found in the usual chips, M/BE utilizes a concept known as Zero-Relative Addressing (ZRA).

ZRA allows all devices and memory regions to be addressed with an offset relative to zero. This allows mitigation and reduction of address fragmentation as well as overlapping memory regions among other things.

(How does it work?)

A physical address is a true memory address that references a location within an address space. Unlike with typical architectures where addresses are truly linear, M/BE encodes physical addresses as such:



M/BE is to implement a Network-on-Chip (NoC) structured in a way such that the region identifier equates to the NoC endpoint/node ID.

Mirocom QXI interconnect

The Mirocom Quick Looped Interconnect (QXI) is the standard for Network-on-Chip interconnects within the Mirocom space.

Terminology

Ringstop:
: A ringstop is an single interconnecting endpoint on a ringbus and is responsible for handling time-division multiplexing of the ingress passdown link and passdown injection to the egress passdown link.

Passdown link:
: A passdown link is an connection that passes through one ringstop to the next, forming a feedback loop that allows the bus to circularly propagate packets.

Passdown injection:
: Passdown injection allows for a node on the bus to inject its own packets into a ringstop.

Architectural overview

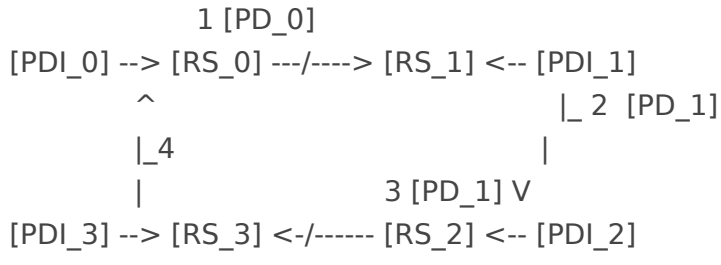
The Mirocom QXI fabric is a high-performance dual ring interconnect that incorporates zero-relative addressing such that each node can be identified with a 5-bit region identifier and addressed with a 27-bit offset, both of which are encoded in a 32-bit physical address. In a typical configuration, one ring will be going clockwise and meant for requests while the other ring goes counter clockwise and meant for data responses.

The QXI fabric is considered a Network-on-Chip that speaks QXI packets. A QXI packet frame encapsulates
metadata such as a CRC32 checksum, sequence number, packet kind, destination node, source node as well
as the packet payload and more.

Physical address format

```
 offset  region
+-------+-----+
| 31:5      | 4:0    |   bits
+-------+-----+
```

High-level diagrammatic representation of a single ring



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Where:

RS_N => Ringstop

PD_N => Passdown link

PDI_N => Passdown link injection